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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte DAVID WILLIAM BOERSTLER, ESKINDER HAILU, KAZUHIKO MIKI and JIEMING QI

Appeal 2011-004190
Application 11/171,758
Technology Center 2800

Before TERRY J. OWENS, HUBERT C. LORIN, and KAREN M. HASTINGS, *Administrative Patent Judges*.

HASTINGS, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants seek our review under 35 U.S.C. § 134 of the Examiner's final decision rejecting claims 9-13, 18-20, 22, and 23. We have jurisdiction over the appeal under 35 U.S.C. § 6(b).

We REVERSE.

Claim 9 is illustrative of the claimed subject matter (emphasis added):

9. A method for translating signals from a first voltage of a first voltage source to a second voltage of a second voltage source, wherein a first level shifter that has an input and an output is connected to the first voltage source, and wherein a second level shifter that has an input and an output is connected to the second voltage source, the method comprising:

receiving, by an intermediate level shifter, an input signal from said first level shifter, said input signal having a first duty cycle and a maximum voltage that is said first voltage, wherein said intermediate level shifter has an input and an output, and further wherein the input of the intermediate level shifter connects to the output of the first level shifter; the output of the intermediate level shifter connects to the input of the second level shifter; and wherein the intermediate level shifter includes an intermediate p-channel transistor and an intermediate n-channel transistor, *and further wherein an intermediate source of the intermediate p-channel transistor is connected to a constant intermediate voltage source having an intermediate voltage about midway between the first voltage of the first voltage source and the second voltage of the second voltage source*; wherein the first voltage is a higher voltage than the second voltage;

shifting, by said intermediate level shifter, said input signal from said first voltage to said intermediate voltage to generate an intermediate signal, wherein said intermediate signal is inverted with respect to said input signal, and wherein positive pulses of said intermediate signal are shrunk and inverted with respect to corresponding pulses of said input signal and negative pulses of said intermediate signal are stretched and inverted with respect to corresponding pulses of said input signal;

receiving, by said second level shifter, said intermediate signal and shifting said intermediate signal to generate an output signal that is inverted with respect to said intermediate signal, said output signal having said first duty cycle and a maximum voltage that is said second voltage; and

wherein the second level shifter includes a first p-channel transistor having a first source that is connected to the second voltage source and a first drain that is connected to a second drain of a first n-channel transistor, and wherein the connection of the first drain of the first p-channel transistor and the second drain of the first n-channel transistor form an output that is

the output signal, and further wherein a second source of the first n-channel transistor is connected to ground, and still further wherein the second voltage source is a constant voltage source.

Independent claim 22 recites a similar method and independent claim 23 recites a similar corresponding circuit.

The Examiner maintains, and Appellants appeal, the following rejections:

Claims 9-11, 18-20, 22 and 23 under 35 U.S.C. § 102(b) as being anticipated by Horiguchi (US 6,046,604 patented April 4, 2000);

Claims 12 and 13 under 35 U.S.C. § 103(a) as unpatentable over Horiguchi in view of Sedra/Smith ("Microelectronic Circuits: 5th Edition" Oxford University Press (C) 2004, pp. 79, Appendix D1-D15, and E1-E4).

PRINCIPLES OF LAW

> [U]nless a reference discloses within the four corners of the document not only all of the limitations claimed but also all of the limitations arranged or combined in the same way as recited in the claim, it cannot be said to prove prior invention of the thing claimed and, thus, cannot anticipate under 35 U.S.C. § 102.

Net MoneyIN, Inc. v. VeriSign, Inc., 545 F.3d 1359, 1371 (Fed. Cir. 2008).

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *See Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631-32 (Fed. Cir. 1987).

"[D]uring examination proceedings, claims are given their broadest reasonable interpretation consistent with the specification." *In re Translogic*

Tech., Inc., 504 F.3d 1249, 1256 (Fed. Cir. 2007), quoting *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000). *See also, In re Am. Acad. of Sci. Tech Ctr*., 367 F.3d 1359, 1364 (Fed. Cir. 2004) (The scope of the claims in patent applications is not determined solely on the basis of the claim language, but upon giving claims their broadest reasonable construction in light of the specification as it would be interpreted by one of ordinary skill in the art.).

ANALYSIS

Appellants argue that the Examiner has not shown how Horiguchi identically discloses that "an intermediate source of the intermediate p-channel transistor is connected to a constant intermediate voltage source having an intermediate voltage *about midway* between the first voltage of the first voltage source and the second voltage of the second voltage source" as recited in independent claim 9 (and in claims 22 and 23) (Br. 8-12). A preponderance of the evidence supports Appellants' position.

Specifically, even assuming that Horiguchi teaches that the intermediate voltage is constant and is in between first and second voltages, the Examiner has not provided any persuasive technical reasoning or evidence that such a voltage is "about midway". Appellants' position is that the "amount of information presented in Horiguchi's Fig. 11B is wholly insufficient" to support the Examiner's findings (Br. 11). A preponderance of the evidence supports Appellants' position that the Examiner's reliance on Fig. 11B is not sufficient to establish anticipation of this feature (Br. 9-12). In this regard, while patent drawings can anticipate claims if the drawings clearly show the claimed structure, *In re Mraz*, 455 F.2d 1069, 1072 (CCPA 1972), patent drawings not designated as being drawn to scale

cannot be relied upon to define precise proportions of elements if the specification is completely silent on the issue. *Hockerson-Halberstadt, Inc. v. Avia Group Int'l, Inc.* 222 F.3d 951, 956 (Fed. Cir. 2000). The Examiner's de facto position that any voltage that is in between two other voltages is a sufficient description of "about midway" so as to anticipate claim 9 (as well as claims 22 and 23) is unreasonable (Ans. 21).

Therefore, we cannot sustain this anticipation rejection.

Accordingly, the Examiner's § 102 rejection is reversed.

The Examiner did not rely upon any other reference or Sedra/Smith to remedy this deficiency. Accordingly, the Examiner's § 103 rejection of claims 12 and 13 is also reversed.

DECISION

We reverse the Examiner's rejection.

ORDER

REVERSED

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